REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections under 35 USC § 112, Second Paragraph

Claims 4, 5, 9 and 10 are rejected under *35* U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse these rejections.

The Examiner has stated that

> "Claim 4 is indefinite because the limitation "the drain terminal of said second transistor is connected to said node" is misdescriptive. Claim 3 recites that "said first current source and said second current source drive said node". The drawings does not show that the current source in the primary current block drives the drain terminal of the second NMOS transistor in the backup current block." (Emphasis added)

Applicants respectfully point to the Examiner that claim 4 does not recite that the primary current block drives the drain terminal of the second NMOS transistor. Claim 4 further defines the secondary current block as shown and described in figure 6. As described, the secondary current block comprises NMOS transistors 630 and 640. The drain terminal of the transistor 640 is connected to the node 512, which is also driven by the primary current source 510 via the current mirror circuit (transistors 610 and 620). Applicants believe that the specification adequately describes the subject matter recited in claim 4. Claim 9 has been rejected in the manor of claim 4, accordingly, claim 9 is also clearly supported by the specification for the same reasons as claim 4. Applicants respectfully request the withdrawal of the rejection of claims 4 and 9 and those dependent thereform under 35 USC §112, second paragraph.

Claim Rejections -35 USC § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935). Applicants respectfully traverse these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 1, the cited reference does not teach or suggest all the claim limitations.

As to claim 1, the Examiner has cited figure 1 of Renous as showing all limitations of claim 1. Applicants respectfully point to the Examiner that figure 1 of Renous describes a circuit whose functionality is in complete contrast to what is recited in claim 1. For example, figure 1 of Renous describes a circuit that will ensure that the node S will always get the largest of the two input voltages V1 and V2 (*see* figure 2 and col. 1, line 30 – col. 2, line 5). In contrast claim 1 distinctly recites that the secondary supply voltage is less than the primary voltage supply and the primary bias current is generated using the secondary voltage supply. Further, claim 2 distinctly recites that the back-up bias current is only used when the second supply voltage is not present, wherein the second supply voltage is less than the first supply voltage. Renous' circuit works in a complete opposite way than what is recited in claim 1.

Further, as to the requirement of the reference must teaching or suggesting all claim limitations, Renous does not teach each and every limitation of claim 1. For example, claim 1 distinctly defines limitations such as:

1. A plurality of transistors of **a low voltage specification**,
2. Circuit portion operating using a first supply voltage, wherein said **first supply voltage is greater than said low voltage specification**,
3. A primary current block generating a primary bias current using a second supply voltage, wherein said **second supply voltage is less than said first supply voltage**;
4. a backup current block generating a **backup bias current using said first supply voltage**.

The Examiner has also stated that Renous does not show any circuit or block for primary and back-up bias generating circuits. Applicants respectfully point to the Examiner that given the specific limitations recited in claim 1 and explained above, Renous does not teach each and every limitation of claim 1 and claim 1 is clearly and patentably distinguishable from Renous.

Claims 2-3 depend from claim 1 and are patentably distinguishable from Rnous for at least the same reasons as claim 1.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935) in view of Yamauchi (USP 5982162). Applicants respectfully traverse these rejections.

Claim 4 recited specific connections of various elements of the second current source. The Examiner has cited figure 3 of Yamauchi as showing the circuit elements recited in claim 4. Further the Examiner has repeated the elements recited in claim 4 as described in figure 3 without providing any reference. For example, the Examiner has stated that the drain terminal of the second NMOS transistor is connected to the node and the source of the second NMOS transistor is connected to the source of the first NMOS transistor, as recited in claim 4. However, a careful examination of figure 3 of Yamauchi reveals that actually both terminals of the second NMOS transistor 31 are connected to ground (one via resistor 27). Thus, Yamauchi describes a completely different circuit with completely different functionality and application than what is recited in claim 4. Accordingly, claim 4 is further patentably distinguishable from the combination of cited references.

Claim *5* is rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935) in view of Yamauchi (USP 5982162) and Wang (USP 5939933). Applicants respectfully traverse this rejection.

Claim 5 depends from claims 1 and 4, which have been distinguished from the combination of Renous and Yamauchi. Accordingly, claim 5 is patentably distinguishable from the combination of cited references for at least the same reasons as claims 1 and 4.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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